Die Cavity Integration Technology for Through-Silicon-Vias Stacking


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Outline

- Introduction -3D Silicon Integration
- 3D Integration Key Technologies
  - Through-Silicon-Via
  - Interconnection
- Die Cavity Integration Technology
  - Wafer-to-wafer and die-to-wafer 3D integration process
  - Fabrication Process Flows
  - Experimental Results & Characterization
- Summary & Conclusions
- Acknowledgements
Emerging 3D Silicon Integration

- **CMOS scaling trend**
  - Performance increase in proportion to the number of transistors.
  - Conventional device scaling is approaching the physical limits.

- **Potential of 3D Integration**
  - To solve interconnect bandwidth
  - Reduced wire delay
  - Increased packaging density
  - Heterogeneous chips
### 3D Silicon Integration Level

<table>
<thead>
<tr>
<th></th>
<th>100</th>
<th>10</th>
<th>1</th>
<th>0.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via &amp; bump size (um)</td>
<td>3D IC</td>
<td>3D IC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3D chip stack</td>
<td>3D chip stack</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Via &amp; bump pitch (um)</td>
<td>3D IC</td>
<td>3D IC</td>
<td>3D IC</td>
<td>3D IC</td>
</tr>
<tr>
<td></td>
<td>3D chip stack</td>
<td>3D chip stack</td>
<td>3D chip stack</td>
<td>3D chip stack</td>
</tr>
<tr>
<td>Silicon thickness (um)</td>
<td>3D IC</td>
<td>3D IC</td>
<td>3D IC</td>
<td>3D IC</td>
</tr>
<tr>
<td></td>
<td>3D chip stack</td>
<td>3D chip stack</td>
<td>3D chip stack</td>
<td>3D chip stack</td>
</tr>
<tr>
<td>Interconnection density (pins/cm²)</td>
<td>3D IC</td>
<td>3D IC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3D chip stack</td>
<td>3D chip stack</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**K. Sakuma, et al., 3D-SIC 2008**
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Through-Silicon-Via (TSV)

- **Fabrication**
  - Copper core TSV
  - Copper filled annular TSV
  - Tungsten filled annular TSV
    - aspect ratio > 30:1

- **Electrical Characteristics**
  - ~10 mohm (50 μm tall)
  - ~40 mohm (150 μm tall)

- **Reliability**
  - 1,000 deep thermal cycles with no increase in resistance or yield loss
  - Current dimension of 200 μm pitch vias can easily carry > 1 Amp

** P. Andry, et al., ECTC 2006
C. Tsang, et al., MRS 2006

25,920 vias probed
Yield = 100%

50um deep tungsten TSV

25,920 vias probed
Yield = 100%

150um deep tungsten TSV
Interconnection

C4 solder interconnect
- Larger spacing between balls and higher joint gaps than low-volume solder interconnect
- >20,000 thermal cycles (stress-free Si-on-Si)

** B. Dang et al., ECTC 2007

Low-volume lead-free solder interconnect
- Relatively low temperature bonding (<300ºC)
- Form an intermetallic phase with a melting temperature much higher than low bonding temperature

** K. Sakuma et al., ECTC 2007, 2008

Copper direct interconnect
- Attractive due to use of Cu in standard CMOS interconnect metallization.
- High thermal conductance and low electrical resistivity.
- Requires optimized Cu surface preparation, high bonding force and elevated temperature.

** K-N. Chen et al., IEDM 2006
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Wafer-to-wafer and die-to-wafer 3D integration process

### Wafer-to-wafer integration

- **Silicon wafer**
- **Top link wafer**
- **TSV carrier wafer**
- **Substrate wafer**

### Die-to-wafer integration

- **CMOS TSV fabrication**
- **Solder fabrication**
- **Sorting Known good die**
- **Stacking**

### Comparison Table

<table>
<thead>
<tr>
<th>Alignment required</th>
<th>Wafer-to-Wafer</th>
<th>Die-to-Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yields</td>
<td>Wafer scale</td>
<td>Die size</td>
</tr>
<tr>
<td>Throughput on stacking</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Suitable for</td>
<td>High</td>
<td>Low</td>
</tr>
<tr>
<td></td>
<td>Common size</td>
<td>Both common and dissimilar size</td>
</tr>
</tbody>
</table>
Die-to-wafer 3D integration with the die cavity technology

- The cavity holds a die and can be used as a positioning reference.

** K. Sakuma, et al., ECTC 2008
Die-to-wafer lamination using the die cavity technology

- All die are bonded simultaneously in the bonding process.

**K. Sakuma, et al., ECTC 2008**
Integration Approach and Test vehicles for 3D Chip Stack

- **Die-to-wafer integration**
  - High flexibility
  - High yield

- **Test Vehicles**
  - Top link wafer:
    - 4-on-8 mil spaced TSV and lead-free solder interconnect
    - Cu wiring
  - TSV carrier:
    - 4-on-8 mil spaced TSV and lead-free solder interconnect
  - Substrate wafer:
    - Cu wiring forms with electroless Ni and immersion Au
    - Large collection of 4 pt. probe taps
Annular metal TSV, lead-free solder interconnect and bonding process flow

(a) Deep Silicon RIE, Insulation, Conductive material fill
(b) Build metal on top
(c) Build wiring levels or BLM pad
(d) Laminate, Expose vias
(e) Backside process Add BLM & Lead-free interconnect
(f) Bonding / Glass release
TSV and Interconnect for 3D Integration

- Annular tungsten TSV and Cu/Ni/In lead-free solder interconnect are demonstrated for 3D integration with the die cavity technology.
Results demonstrated initial feasibility for stacking dies with 200-μm pitch interconnections.
Non destructive X-ray image and cross-sectional SEM image of 3D Chip Stack

- The three layers are vertically stacked and connected by TSVs and lead-free solder interconnects.
- Each stacked chip thickness is approximately 70 μm.
Electrical characterization of multi layer chip stack

- Average resistance of a single tungsten TSV and Cu/Ni/In solder interconnect was approximately 21 mΩ.
Thermal reliability of stacked chip

Reliability test conditions

<table>
<thead>
<tr>
<th>Test item</th>
<th>Test condition</th>
</tr>
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<tbody>
<tr>
<td>Preconditioning (JEDEC level-3)</td>
<td>125°C C bake for 24hrs, 30°C /60% RH for 192hrs, and three times 260°C peak</td>
</tr>
<tr>
<td></td>
<td>reflow</td>
</tr>
<tr>
<td>Thermal Cycling test</td>
<td>-55°C C to +125°C, 1,000 cycles</td>
</tr>
</tbody>
</table>

Chain yields at a total of 84 different locations on three stack samples through deep thermal cycling and Mean resistances and standard deviations of the chains after 1,000 thermal cycles

<table>
<thead>
<tr>
<th>Sample</th>
<th>Chain yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 cycle</td>
</tr>
<tr>
<td>No.1</td>
<td>98.8</td>
</tr>
<tr>
<td>No.2</td>
<td>98.8</td>
</tr>
<tr>
<td>No.3</td>
<td>100</td>
</tr>
</tbody>
</table>

** K. Sakuma, et al., ECTC 2008
Summary and Conclusions

- A Die-to-wafer integration using the die cavity process was demonstrated.
- 6-layer chip stacks on silicon substrates were produced by using the die cavity process.
- Electrical resistance measurements revealed a combined single via plus bump resistance as low as 21 mΩ, which is a suitable for high performance system.
- No yield loss after 1,000 deep thermal cycles with initial good junctions without underfilling.
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