3D Through Silicon Stacking for Mobile/Wireless Markets – Gaps and Challenges

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Mobile/ Wireless Market Drivers

1G  2G  3G & Beyond

Mobile Communication + Information + Entertainment / CE + Rich Communication + User Generated Content/ Social Networking + Computing

PHONE EVOLUTION

Handset market ~ 1.4B/year

Pocketable Computing Devices

Laptop market ~ 200M/year
Why 3D Through Silicon Stacking for Mobile/Wireless Products?

- Today, QCOM addresses this market with stacked bare die using wirebond and flip chip.
- With exploding wireless mobile applications for compute, video, gaming, & MM, **power efficient performance** becomes a key challenge.
- **Reduction in cost per function** is increasingly difficult as we reach the limits of Moore’s Law scaling.
- “More than Moore” solutions needed. 3D TSS as key technology platform for MtM.
Thru Silicon Stacking (TSS)

Value Propositions

- **Package Density**
  - very thin die stacking

- **Improved Performance**
  - shorter electrical paths
  - reduced power

- **New architectural and partitioning capabilities**
  - extreme chip to chip bandwidth
  - choose optimum node/material for each block of the design
## Qualcomm TSS Roadmap

<table>
<thead>
<tr>
<th>STAGE</th>
<th>TSV</th>
<th># TIERS</th>
<th># VIAS</th>
<th>VIA DIA/DEPTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAGE1</td>
<td>Cu after FEOL</td>
<td>ITRS (2010-2012) Via dia: 2-2.5um Depth: 10-15um</td>
<td></td>
<td>6um/50um</td>
</tr>
<tr>
<td>STAGE2</td>
<td>Cu via after FEOL</td>
<td>2-3</td>
<td>10,000s</td>
<td>2-3um/25um</td>
</tr>
<tr>
<td>STAGE3</td>
<td>Cu via after FEOL</td>
<td>3 or more</td>
<td>&gt;</td>
<td>&lt;2-3um/&lt;25um</td>
</tr>
</tbody>
</table>
Key Challenges and Gaps

- Technical
- Manufacturability
- Supply Chain
- Product Adoption
Technical Challenges & Gaps

- **Process equipment and materials**
  - thin wafer handling and temporary wafer glue
  - high throughput P&P/low temp fine pitch bond & underfill
  - low temp RDL-B dielectric
  - compatibility with advanced CMOS materials: ultra low K, etc

- **EDA tools and flows**
  - Tier-aware extraction, DRC, LVS, tech files
  - 3D power grid and signal Integrity optimization tools
  - Thermal-awareness
  - Floorplanning, P&R, timing

- **Test/ DFT**
  - test strategy and circuits
  - PGD → KGD
  - failure analysis techniques
Manufacturability Gaps

- **Processing Cost**
  - cost will ultimately be the primary factor dictating industry adoption of TSS in volume products

  - Cost reduction opportunities:
    - equipment/process/materials/flow
    - design techniques
    - die size reduction
    - low density functions in less expensive silicon
    - reduce # metal layers
    - reduce package cost
    - etc.

Manufacturing Cost Model

- TSV
- Top metal/Ship
- Bump
- Microbump
- Assembly

Needs Calibration
More Manufacturability Gaps

- **300mm via-first TSS fab & assembly capability**

- **Yield**
  - lack of manufacturing-level yield demonstrations on advanced CMOS nodes
  - variation control

- **Qualification**
  - reliability data and characterization on leading edge tech node

- **Metrology**
  - TSV size/depth/profile/fill
Supply Chain Challenges
“Post-FAB Wafer Processing”

Wire Bond
- FAB: Fab → Probe
- SAT: Asy → Test

Flip Chip
- FAB: Fab → Bump → Probe
- SAT: Asy → Test

Via-First TSS
- FAB: TSV_F → Fab → Bump → Probe → TSS_F
- SAT: Asy → Test

TSS_F includes temp wafer bond/debond, thin, RDL-B, uBump, DtW attach
Supply Chain Challenges

- **Division of responsibilities**
  - fabs, SATS, consortia, equip’t vendors
  - equipment investment for “post fab wafer processing”
  - development and pre-production costs
  - process integration responsibility
  - lead customers

- **Cost impact of process flow & supply chain**

- **Multisourcing**

- **Lack of standards, infrastructure**
  - Interfaces, flows
Product Adoption Challenges “crossing the chasm” - Geoffrey Moore

- COO forecasts for \textit{predictive} cost modeling
- Risk mitigation
  - test chips, reliability data, volume demos
- System-level benefit analysis
  - quantify value proposition
- Lead product selection
  - TSS critical, fail safe
- Tools for “Pathfinding” tradeoff studies
3D TSV Chip Stacking Choices

**Process Technology “Knobs”**
- Bonding & Redistribution
  - Via First or Via Last
  - Wafer to Wafer or Die to Wafer
- Through Si Via
  - Size, Density & Keep Out Area
  - Metal Fill, liner thickness
- Number & Sequence of Tiers
  - 2 or more
  - Face to Face or Face to Back
  - Technology node for each tier

**Design Architecture “Knobs”**
- Stacking (mostly) Existing Die
  - e.g. Memory on Logic
  - e.g. Analog on Logic
- Stacking Purpose-Designed Die
  - e.g. Wide Bandwidth Memory
  - e.g. Partitioned Logic
- Managing Architectural Options
  - Bandwidth and Latency
  - Clock Skews and Variability
  - Test/DFT, thermal effects

Finding the Right Mix requires Exploratory Designs = PathFinding
Product Adoption for Disruptive Advanced Technology

- How to connect a Technology Concept with real, in-product, implementation

**PathFinding**
(virtual design)

- Explore design and architecture possibilities that leverage a given technology opportunity
- Address risk concerns early enough and well enough to attract product teams towards exploiting the technology
- Concurrently tune architecture and process for target product

**Validation**
(methodologies, tools, test chips)

**Adoption**
(product implementation)

Tech Concept

- System Level PathFinding Environment (virtual)
- Virtual Chip Architecture
  - Virtual RTL
  - Virtual Synthesis
  - Virtual NEL/LAT
- Virtual Physical Design
  - Virtual SoC
- Virtual Technology Enablement
  - Virtual Lib
  - Virtual LEF
- Legacy Component Models
e.g. modem, GU, memories, ...
- Technology Input Estimates
- Output Estimates
  - COST
  - POWER
  - TIMING
- Software Models
- Physical Layout
  - Model e.g. shrink factors
- Electrical Device
  - Model e.g. PTM
Pathfinding Virtual Chip Design Flow

- **Output Estimates**
  - COST
  - POWER
  - TIMING

- **Virtual Chip Architecture**
  - Virtual RTL

- **Virtual Synthesis**
  - Virtual NETList

- **Virtual Physical Design**
  - Virtual SoC

- **Virtual Technology Enablement**
  - Virtual .lib ➔ Virtual LEF

- **Virtual Component Models**
  - e.g.: modem, GU, memories, ...
  - w/ variability ➔ nominal

- **Technology Input Estimates**
  - Physical Layout Model ➔ e.g., shrink factors
  - Electrical Device Model ➔ e.g., PTM, ...

- **System Level PathFinding Environment**

- **Legacy Component Models**

- **Legacy data**

- **Software Models**
Virtual Chip Design Flow
Architecture/3D TSS Exploration

Software Models

System Level PathFinding Environment
Platform Requirements
- use cases
- activity factors
- cost/performance/power targets

Architectural Choices
- component selection
- bus architecture
- functional partitioning

Virtual Chip Architecture
Virtual RTL

Virtual Synthesis
Virtual NETLsit

Virtual Physical Design
Virtual SoC

Output Estimates
COST POWER TIMING

Electrical Device Model
- e.g. PTM, .....

Technology Input Estimates
Physical Layout Model
- e.g. shrink factors

Virtual Technology Enablement
- nomimal

Virtual Component Models
- e.g: modem, GU, memories, ..
Conclusions

- 3D TSS will be utilized for wireless/mobile applications enabling new architectures and partitions with significant improvement in power efficient performance.

- Cost reduction is critical to volume market application and needs to be better understood and driven.

- There are many technical and business challenges & gaps to achieving productization of TSS. A roadmap with staged evolution is planned.

- Pathfinding tools/methodologies and test chip demos are being utilized to facilitate product adoption.